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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,641	07/27/2004	Kerry Bernstein	HER0101-01	4327
7590 Anthony Niewyk, Esq. BAKER & DANIELS LLP 111 East Wayne Street, Suite 800 Fort Wayne, IN 46802			EXAMINER WHITE, DYLAN C	
			ART UNIT 2819	PAPER NUMBER
			MAIL DATE 06/12/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/710,641

Applicant(s)

BERNSTEIN ET AL.

Examiner

Dylan White

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 July 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 and 10-20 is/are rejected.
- 7) ☒ Claim(s) 9 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 July 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "16" and "28" of Figure 1 have both been used to designate the interconnecting gate where that interconnecting gate is an AND gate. The Examiner suggests that 28 point to a dotted circle around logic gates 30 & 32 which designate the AND gate, where the box designated by 16 can remain the interconnecting gate. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 4-8, 10-15, and 17-20 rejected under 35 U.S.C. 102(b) as being anticipated by Hill et al. (U.S. Pub. 2003/0042933).

Regarding claim 1, Hill discloses at least two redundant dynamic logic gates (102 @ Fig. 1), each dynamic logic gate (left and right) outputting one of a first logic state (0) and a second logic state (1), the second logic state being output in response to a logic input signal (A & B); and an interconnecting gate (104) coupled to an output (C & CN) of each redundant dynamic logic gate (left and right), the interconnecting gate (104) outputting the second logic state (1) only when all of the redundant logic gates (left and right) output the second logic state (1, AND gate will only output a 1 when both C & VN are 1. par. 0008, lines 9-11).

Regarding claim 2, Hill discloses wherein the interconnecting gate (104) includes an AND gate (par 0008, lines 9-11).

Regarding claim 4, Hill discloses wherein each dynamic logic gate (102, left and right) includes a combinatorial logic section (transistors with gate inputs A & B), a pre-charge section (PMOS transistors connected to CK), and an inverting gate (NMOS connected to CK and logic transistor connected to B) positioned downstream (Fig. 1) of a node (between pre-charge PMOS and logic transistor connected to A) connecting the combinatorial logic section (transistors with gate inputs A & B) and the pre-charge section (PMOS connected to CK).

Regarding claim 5, Hill discloses wherein the pre-charge section includes a pre-charge device (PMOS connected to CK) and a keeper device (PMOS connected to inverter output).

Regarding claim 6, Hill discloses wherein an output of the inverting gate (Inverter not labeled) feeds back to the keeper device (PMOS connected to output of inverter).

Regarding claim 7, Hill discloses wherein the interconnecting gate includes a NOR gate (par. 0008, lines 11-15).

Regarding claim 8, Hill discloses wherein each dynamic logic gate (102, left and right) includes a combinatorial logic section (transistors with gate inputs A & B) and a pre-charge section having a pre-charge device (PMOS connected to CK) and a keeper device (PMOS connected to output of inveter).

Regarding claim 10, Hill discloses wherein the fault is a negative fault (par. 0005, lines 1-2).

Regarding claim 11, Hill discloses wherein the interconnecting gate is a static gate (104).

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Regarding claim 12, Hill discloses wherein each dynamic logic gate is a cascode voltage switch (par. 0002, lines 2-4).

Regarding claim 13, Hill discloses first means (102, left side) for outputting one of a first logic state (0) and a second logic state (1), the second logic state being output in response to a logic input signal (inputs A & B); second means (102, right side) for outputting one of the first logic state (0) and the second logic state (1), the second logic state being output in response to the logic input signal (inputs A & B); and third means for interconnecting outputs (104, par. 0008, lines 9-11) of the first means and the second means (102, left and right, respectively), and for correcting a fault by outputting the second logic state (1) only when both the first means (102, left side) and the second means (102, right side) output the second logic state (1).

Regarding claim 14, Hill discloses providing a first dynamic logic gate (102, left side); providing a second dynamic logic gate (102, right side) that is redundant to the first dynamic logic gate (identical structure); and combining outputs of the first (C) and second (CN) dynamic logic gates (102) to correct a fault in one of the first dynamic logic gate and the second dynamic logic gate (par. 0005, lines 1-2).

Regarding claim 15, Hill discloses wherein the combining step (@ logic 104) includes interconnecting outputs of the first (C) and second (CN) dynamic logic gates with an AND gate (par. 0008, lines 9-11).

Regarding claim 17, Hill discloses wherein the combining step (@ logic 104) includes interconnecting outputs of the first (C) and second (CN) dynamic logic gates with a NOR gate (par. 0008, lines 11-15).

Regarding claim 18, Hill discloses wherein each dynamic logic gate (102 left and right) is a cascode voltage switch (par. 0002, lines 2-4).

Regarding claim 19, Hill discloses wherein the fault is a soft error (par. 0005, lines 1-2).

Regarding claim 20, Hill discloses wherein the combining step includes interconnecting outputs (@ logic 104) of the first and second dynamic logic gates (102, left and right) with a static gate (104).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3 and 16 rejected under 35 U.S.C. 103(a) as being unpatentable over Hill et al. (U.S. Pub. 2003/0042933).

Regarding claim 3 and 16, Hill discloses the logic gate (104) comprising an AND gate (par. 0008, lines 9-11), however fails to disclose where the AND gate is constructed of an NAND gate and an inverter.

The Examiner takes official notice that it notoriously well known and obvious to one of ordinary skill in the art at the time of invention to construct an AND gate out of a NAND gate and an inverter as they are equivalent circuits.

Allowable Subject Matter

Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 9, where the output of the NOR gate feeds back to the keeper device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dylan White whose telephone number is (571) 272-1406. The examiner can normally be reached on m-f 7:30- 4:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DW

Rexford Barnie
REXFORD BARNIE
SUPERVISORY PATENT EXAMINER
06/08/07